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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/858,397	05/16/2001	Frank Randolph Bryant	92-C-074D3 (STMI01-00024)	4170
30425	7590	01/04/2007	EXAMINER	
STMICROELECTRONICS, INC. MAIL STATION 2346 1310 ELECTRONICS DRIVE CARROLLTON, TX 75006			DUONG, KHANH B	
			ART UNIT	PAPER NUMBER
			2822	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		01/04/2007	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/858,397	BRYANT
	Examiner Khanh B. Duong	Art Unit 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 06 October 2006.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 17-23,25,46-49 and 51-59 is/are pending in the application.
- 4a) Of the above claim(s) 17-23,25,58 and 59 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 46-49 and 51-57 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) Notice of Informal Patent Application
- 6) Other: \_\_\_\_\_.

**DETAILED ACTION**

**Response to Amendment**

This office action is in response to the amendment filed October 6, 2006.

Accordingly, claim 46 was amended. Claim 50 was previously canceled.

Claims 17-23, 25, 58 and 59 remain withdrawn from consideration as being directed to a non-elected invention.

Currently, claims 46-49 and 51-57 remain active.

***Response to Arguments***

Applicant's arguments with respect to the amended claims will be addressed in the following new ground(s) of rejection.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 46, 48, 49, 51, 52, 54 and 55 are rejected under 35 U.S.C. 102(b) as being anticipated by “Fabrication Technique for Fully Recessed Oxide Isolation”, IBM Technical Disclosure Bulletin, March 1, 1977, Volume No. 19, Issue No. 10, page 3947-3950.**

Re claims 46, 48, 49 and 54, the IBM Technical Disclosure Bulletin above (herein “IBM TDB”) expressly discloses in FIGs. 2A-2C an integrated circuit device comprising: a substrate (P-Si); a gate structure, wherein the gate structure includes: a gate oxide layer (“OXIDE”) on the substrate; a nitride layer (“NITRIDE”) over the gate oxide layer; and a polysilicon layer

("POLYSILICON") over the nitride layer; a channel region inherently under the gate structure; and source/drain regions (boron ions implanted regions) in the substrate adjacent the channel region; wherein the gate structure has a peripheral edge and further including an uplift (bird's beak) in portions of the nitride layer proximate the peripheral edge of the gate structure. The IBM TDB expressly discloses in FIG. 2C that the nitride layer encasing the polysilicon layer acts as a protective layer and prevents the formation of asperities in the polysilicon layer, including a bottom surface thereof, during a reoxidation step to form recessed oxides.

Re claims 51 and 52, the IBM TDB expressly discloses in FIG. 2C: the substrate has a surface and further including an indentation in the surface of the substrate located proximate to the peripheral edge of the gate structure; the gate structure includes sidewall spacers (NITRIDE) located on each edge of the gate structure and lightly doped drain regions (boron ions implanted regions) in the substrate below the sidewalls spacers.

Re further claims 46, 49, 51, 54 and 55, the claims recite the following product-by-process limitations: the uplift caused by reoxidation of the polysilicon layer within the gate structure; the nitride layer is formed by nitrogen implantation to form an implanted area and by annealing of the implanted area; the uplift caused by reoxidation of the gate structure, wherein asperities are absent from the polysilicon layer; the indentation resulting from reoxidation of the gate structure; and the source/drain regions are implanted prior to or after reoxidation. However, these limitations have not been given patentable weight because product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does

not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

**Claims 46-49, 52, 53 and 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. (U.S. 4,192,059) in view of the IBM TDB.**

Re claims 46, 48, 49, 52, 53 and 55 Khan et al. ("Khan") discloses in FIG. 12 an integrated circuit device comprising: a substrate 3 (p-type); a gate structure, wherein the gate structure includes: a gate oxide layer 4 on the substrate 3; a nitride layer 5 over the gate oxide layer 4; and a polysilicon layer 15 over the nitride layer 5; a channel region under the gate structure; source/drain regions (n-type) in the substrate 3 adjacent the channel region; and

sidewall spacers 34 located on each edge of the gate structure and lightly doped drain regions in the substrate below the sidewalls spacers 34.

Re further claim 46, Khan fails to disclose the gate structure further including an uplift in portions of the nitride layer proximate the peripheral edge of the gate structure, wherein asperities are absent from a bottom surface of the polysilicon layer.

The IBM TDB expressly shows in FIG. 2C, as previously discussed above, the gate structure further including an uplift (bird's peak) in portions of the nitride layer ("NITRIDE") proximate the peripheral edge of the gate structure, wherein asperities are absent from a bottom surface of the polysilicon layer.

Since Khan and the IBM TDB are from the same field of endeavor, the purpose disclosed by the IBM TDB would have been recognized in the pertinent prior art of Khan

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the device disclosed by Khan as taught by the IBM TDB because of the desirability to suppress oxidation at the end of the polysilicon gate.

Re further claims 46, 49, 53 and 55, the claims recite the following process limitations: the uplift caused by reoxidation of the polysilicon layer within the gate structure; the nitride layer is formed by nitrogen implantation to form an implanted area and by annealing of the implanted area; the source/drain regions are formed by implanting n-type impurities in the p-type substrate; and the source/drain regions are implanted after reoxidation. However, the method of forming a device is not germane to the issue of patentability of the device itself. Therefore, these limitations have not been given patentable weight.

Re further claims 47, 56 and 57, Khan fails to show specific dimensional parameters of the nitride layer, gate oxide layer and channel region.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Khan by selecting such dimensional parameters within the ranges as required by the claims, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

### ***Conclusion***

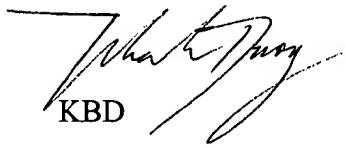
Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

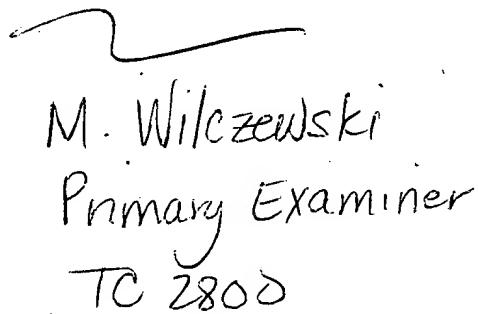
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on Monday - Friday (9:00 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
KBD

  
M. Wilczewski  
Primary Examiner  
TC 2800